FYBSC CS/SEM I/ATKT/Digital System and Architecture

Time: 1 hr. Marks:30

Note:
1. All questions are compulsory.
2. Draw neat diagrams wherever necessary.
3. Figures to the right indicate full marks.

Q.1 **Answer the following. (Any TWO)** [10]

(a) Describe 2:1 multiplexer.
(b) Write a note on Half adder.
(c) Solve using K map: y = ∑m (1,2,3,5,6,7,11,12,13,15)
(d) Draw AND, OR gates using NAND gate.

Q.2 **Answer the following. (Any TWO)** [10]

(a) Find the page Hit and Page miss for the following string using FIFO & LRU page replacement polices considering a frame size three.
2 , 3 , 3 , 1 , 5 , 2 , 4 , 5 , 3 , 2 , 5 , 2
(b) Explain flag register of microprocessor with respect to either 8085 or 8086.
(c) What is addressing mode? Explain any two in detail.
(d) Explain what is Instruction cycle. (diagram is mandatory)

Q.3 **Answer the following. (Any TWO)** [10]

(a) Explain half subtractor with rules, truth table, description and circuit diagram,
(b) Draw and explain D flip flop.
(c) Explain any three Logical instructions.
(d) Draw architecture of Microprocessor (Take reference of 8085).