FYCS/SEM I/REG/DSA

Time: 2½ hrs. **Marks:75**

Note:
1. All questions are compulsory with internal choice.
2. Draw neat diagrams wherever necessary.
3. Figures to the right indicate full marks.

Q.1 Answer the following (any four) **(20)**

(a) Explain NOT, AND and OR gate with their symbol , truth table.
(b) Explain De-Morgan's theorem.
(c) Using NOR gate draw NOT , AND and OR gate.
(d) Draw IC diagram of NOR gate and NAND gate.
(e) Draw the circuit diagram for following Boolean expression.
i. $\bar{A}B + \bar{A}\bar{B}$
ii. $\bar{A} + BC + \overline{(BC)}$
(f) Simplify using K-map :y=∑m(1,3,5,7,12,14)

Q.2 Answer the following (any four) **(20)**

(a) Explain memory hierarchy in detail.
(b) What is addressing mode? Explain any three addressing modes.
(c) Explain data transfer techniques of DMA.
(d) Processor requires the pages from virtual memory in the following sequence: 2,3,2,1,5,2,4,5,3,2,5,2 calculate Hit and Miss ratio using FIFO and LRU.
(e) Explain daisy chaining and polling methods of Bus Contention.
(f) Write a note on virtual memory management using paging.

Q.3 Answer the following (any four) **(20)**

(a) Write micro operations for ADD BL,25 and MOV BL,[BX]
(b) Draw and Explain instruction cycle.
(c) Explain delay element method with advantages and disadvantages.
(d) Explain Wilke's design for a Microprogrammed control unit.
(e) Differentiate between SRAM and DRAM.
(f) Explain memory interleaving.

Q.4 Answer the following (any five) **(15)**

(a) Simplify using K-map : y=∑m(0,2,5,8,10,13)
(b) Explain 4:1 multiplexer.
(c) Explain Flynn's Classification of parallel Computing.
(d) Explain Half adder with circuit diagram, symbol and truth table.
(e) Processor requires the pages from virtual memory in the following sequence: 7,5,3,2,1,0,4,1,6,7,4,2 calculate Hit and Miss ratio using FIFO and LRU.
(f) Design a 3-bit asynchronous up-counter by using JK flip-flops.

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