FYIT/SEM I/REG/DLA

**Time: 2½ hrs.** **Marks:75**

**Note:**
1. All questions are compulsory with internal choice.
2. Draw neat diagrams wherever necessary.
3. Figures to the right indicate full marks.

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**Q.1 Answer the following (any three)** **(15)**

**(a)** Convert :

i) $(126)_{10}$ to ( ? )$_2$

ii) $(127)_8$ to ( ? )$_2$

**(b)** Solve using 1's complement.

i) 12 - 10 ii) 12 - 13

**(c)** Multiply :

i) (1101) x (111)
ii) (1110) x (110)

**(d)** Convert in to BCD :

i) $(26)_{10}$
ii) $(52)_{10}$

**(e)** Perform :

i) (1101111) + (111010)
ii) (1111001) - (100101)

**(f)** Convert :

i) $(79)_{10}$ to ( ? )$_2$
ii) $(DB)_{16}$ to ( ? )$_2$

**Q.2 Answer the following (any three)** **(15)**

**(a)** Explain with the help of circuit diagram how NAND gate is used to create NOT, AND and OR gate?

**(b)** Describe XNOR and NOR gate with Symbol, Truth table, Boolean expression and Waveform.

**(c)** Draw the circuit diagram for following Boolean expression.

*i.* $\overline{AC}\,B + \bar{A}\bar{B}C$

*ii.* $\bar{B} + B + \overline{(AB)}$

**(d)** Explain Demorgan's laws.

**(e)** Draw EXOR gate using NAND gate and then using NOR gate.

**(f)** Simplify using K-map : $y=\sum m(1,2,9,10,11,14,15)$

**Q.3 Answer the following (any three)** **(15)**

**(a)** Explain half subtractor in detail.

**(b)** Explain 1 bit comparator.

**(c)** Simplify using multiplexer : $y=\sum m(1,2,4,6,7)$

**(d)** Explain 4:1 multiplexer.

**(e)** Design 16:1 multiplexer using 8:1 multiplexer.

**(f)** Explain full adder in detail.

**Q.4** **Answer the following (any three)** **(15)**

(a) Explain R-S flip flop with circuit diagram and truth table.

(b) Explain J-K flip flop with circuit diagram and truth table.

(c) Solve using K map : $y=\sum m(0,2,5,6,7,8,10,13,15)$.

(d) Draw full adder using multiplexer.

(e) Draw full subtractor using multiplexer.

(f) Explain D flip flop in detail.

**Q.5** **Answer the following (any three)** **(15)**

(a) Explain 3 bit asynchronous up counter.

(b) Design MOD 9 counter.

(c) Explain ALU in detail.

(d) Design MOD 12 counter.

(e) Explain 3 bit asynchronous down counter.

(f) Explain serial in serial out shift register.

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