FYCS/SEM I/DSA

A (1)

Time: 2½ hrs. **Marks:75**

Note:
1. All questions are compulsory with internal choice.
2. Draw neat diagrams wherever necessary.
3. Figures to the right indicate full marks.

Q.1 Answer the following (any four) **(20)**

(a) Explain NOT , AND and OR gate with their symbol , truth table.

(b) Explain both the Demorgan's law.

(c) Using AND gate draw NOT , AND and OR gate.

(d) Draw IC diagram of AND gate and NAND gate.

(e) Draw the circuit diagram for following Boolean expression.

i. $\bar{A}B + \bar{A}\bar{B}$

ii. $\bar{A} + BC + \overline{(BC)}$

(f) Simplify using K-map : $y=\sum m(0,2,5,8,10,13)$

Q.2 Answer the following (any four) **(20)**

(a) Explain memory hierarchy in detail.

(b) What is addressing mode? Explain any three addressing modes.

(c) Write a note on pipelining.

(d) Processor requires the pages from virtual memory in the following sequence:
2,3,2,1,5,2,4,5,3,2,5,2 calculate Hit and Miss ratio using FIFO and LRU techniques.

(e) Explain Daisy Chaining and Polling methods of Bus Contention.

(f) Write a note on virtual memory management using Pagging.

Q.3 Answer the following (any four) **(20)**

(a) Write micro operations for MOV BL,25 and ADD BL,CL

(b) Draw and Explain instruction cycle.

(c) Explain Delay Element Method with advantages and disadvantages.

(d) Explain Wilke's design for a Microprogrammed control unit.

(e) Differentiate between Memory mapped I/O and I/O mapped I/O.

(f) Explain memory interleaving.

Q.4 Answer the following (any five) **(15)**

(a) Simplify using K-map : $y=\sum m(0,2,5,8,10,13)$

(b) Explain 4:1 multiplexer.

(c) Implement using multiplexer : $y=\sum m(0,2,5,8,10,13)$

(d) Explain Half adder with circuit diagram, symbol and truth table.

(e) Processor requires the pages from virtual memory in the following sequence:
7,5,3,2,1,0,4,1,6,7,4,2 calculate Hit and Miss ratio using FIFO and LRU techniques.

(f) Write micro operations for MOV CL,25 and SUB BL,CL.